ABSTRACT

A die is formed with different and optimized critical dimensions in different device levels and areas of those device levels using photolithography and etch techniques. One aspect of the invention provides for a memory array formed above a substrate, with driver circuitry formed in the substrate. A level of the memory array consists of, for example, parallel rails and a fan-out region. It is desirable to maximize density of the rails and minimize cost of lithography for the entire memory array. This can be achieved by forming the rails at a tighter pitch than the CMOS circuitry beneath it, allowing cheaper lithography tools to be used when forming the CMOS, and similarly by optimizing lithography and etch techniques for a device level to produce a tight pitch in the rails, and a more relaxed pitch in the less-critical fan-out region.